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Inventor(s):

Filing Date:

Title:

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Typed Name: Nichael G. Verga

PATENT APPLICATION

ATTORNEY DOCKET NO. 200207855-1

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Group Art Unit:

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Date: 10/13/03

Telephone No.: (617) 439-2871

Examiner: Not assigned

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Benjamin T. Percer and Andrew M. Cherniski

COMPUTER DATA BUS INTERFACE CONTROL

PO Box 1450 Alexandria, VA 22313-1450	
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This Information Disclosure Statement is submitted:	
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			APPLICANT	First Named Inventor	Benjamin Thomas Percer, et al.
				Art Unit	Not Yet Assigned
(Use as many sheets as necessary)		Examiner Name	Not Yet Assigned		
Sheet	1	of	1	Attorney Docket Number	200207855-1

			U.S. PA	TENT DOCUMENTS	
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	CA	"Bus Switch Undershoot Protection: Which Systems Need this Protection and Why", FAIRCHILD SEMICONDUCTOR CORPORATION, Application Note AN-500498, pgs.1-3 (2000);	
	СВ	"FSTU – Undershoot Protected Fairchild Switch Family", FAIRCHILD SEMICONDUCTOR CORPORATION, Application Note AN-500222, pgs.1-4 (2000);	
	cc	"FSTU32160 16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch with2V Undershoot Protection", FAIRCHILD SEMICONDUCTOR CORPORATION, Application Note DS500244, pgs.1-6 (2000);	
	CD	"Intel NetStructure ZT 4901 I/O Mezzanine Expansion Card" INTEL CORPORATION, Product Brief, pgs.1-4 (2002);	
	CE	"cPB-4321 PlexSys Family System Master Processor Board", DIVERSIFIED TECHNOLOGY, INC., Configuration Guide Rev 1.6, pgs.1-14 (2002).	

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